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Specification

1. Title of the invention: Manufacturing method of color liquid crystal display device

2. What is claimed is:

1) In a manufacturing method of a color liquid crystal display device with a green color filter, a manufacturing method of a color liquid crystal display device wherein a dyeing base material is dyed with a cyan dye, thereafter said green color filter is dyed by dyeing said dyeing base material with a yellow dye.

3. Detailed description of the invention

[Field of the invention]

The present invention relates to a manufacturing method of a color liquid crystal display device, particularly a manufacturing method of a color liquid crystal display device of an active matrix system using a thin film transistor etc.

[Prior Art]

A liquid crystal display device of an active matrix system is provided with nonlinear elements (switching elements) corresponding to a plurality of pixel electrodes arranged in matrix shape respectively. Because liquid crystal in each pixel is always driven (duty ratio 1.0) in theory, time divisional driving system is adopted. The active matrix system has a fine contrast compared with the so-called simple matrix system so that it is the essential technology especially in a color liquid crystal display device. A typical switching element is a thin film transistor (TFT).

In the conventional manufacturing method of a color liquid crystal display device, a green color filter is dyed with the mixed dye of a cyan dye and a yellow dye.

A liquid crystal display device of an active matrix system using a thin film transistor is known by, for instance, "12.5-inch active matrix system color liquid crystal display with redundant constitution" on page 193 to 210 in Nikkei Electronics, on December 15, 1986, published by Nikkei McGrow Hill.

[Problems to be solved]

However, in a manufacturing method of such color liquid crystal display device, because a slight difference of a dyeing condition affects fluid state of the mixed dye for a dyeing base material, it is difficult that a green color filter is dyed to a prescribed color tone.

This invention is performed to resolve said problem, and has a purpose to offer a manufacturing method of a color liquid crystal display device dyeing a green color filter easily to a prescribed color tone.

[Means for resolving problems]

To achieve this purpose in the present invention, in a manufacturing method of a color liquid crystal display device with a green color filter, a dyeing base material is dyed with a cyan dye, said green color filter is dyed by dyeing said dyeing base material with a yellow dye.

[Effect]

In this manufacturing method of a color liquid crystal display device, each dye receptivity of a cyan dye and a yellow dye for a dyeing base material can be constant by fixing each dyeing condition of the cyan dye and the yellow dye.

[Embodiment]

The following is an explanation of an active matrix system color liquid crystal display device wherein the present invention is applied.

In addition to it, in all Figures for explaining the liquid crystal display device, the same numbers are added to the same functions, and the repeated explanation is omitted.

Figure 2A is a plan view that shows one pixel and its periphery of the active matrix system color liquid crystal display device wherein the present invention is applied. Figure 2B shows a cross section on the cutting line ⅡB-ⅡB in Figure 2A, and a cross section near a seal portion of a display panel. Figure 2C is a cross sectional view on the cutting line ⅡC-ⅡC in Figure 2A. Figure 3 (a plan view of a main portion) shows a plan view wherein a plurality of pixels shown in

Figure 2A are provided.

《Provision of pixels》

As shown in Figure 2A, each pixel is provided in a region (in the region surrounded with four signal lines) where the adjacent two scanning signal lines (a gate signal line or a horizontal signal line) GL and the adjacent two image signal lines (a drain signal line or a vertical signal line) DL cross each other. Each pixel contains a thin film transistor TFT, a transparent pixel electrode ITO1 and a storage capacity element Cadd. The scanning signal line GL extends in the direction of row, and a plurality of those are provided in the direction of line. The image signal line DL extends in the direction of line, a plurality of those are provided in the direction of row.

《Whole structure of cross section in display portion》

As shown in Figure 2B, a liquid crystal LC is provided as a base. A thin film transistor TFT and a transparent pixel electrode ITO1 are formed on a lower transparent glass substrate SUB1, and a color filter FIL and a shielding film BM forming a black matrix pattern for shielding are formed on a upper transparent glass substrate SUB2. The thickness of the lower transparent glass substrate SUB1 is approximately 1.1[mm], for instance.

The central part of Figure 2B shows a cross section of one pixel. The left side shows a cross section of the portion wherein an outer leading interconnection exists in the left edge of the transparent glass substrates SUB1 and SUB2. The right side shows a cross section of the portion wherein the outer leading interconnection does not exist in the right edge of the transparent glass substrates SUB1 and SUB 2.

A sealing material SL shown in each left side and right side of Figure 2B is constituted to seal the liquid crystal LC, and is formed along a whole peripheral edge of the transparent glass substrates SUB1 and SUB 2 except an inlet for liquid crystal (not shown in Figure). The sealing material SL is formed by epoxy resin, for instance.

A common transparent pixel electrode ITO2 on the upper transparent glass substrate SUB2, at least in one point, is connected to the outer leading interconnection formed on the lower transparent glass substrate SUB1 by silver paste material SIL. This outer leading interconnection is formed in the same manufacturing process as a gate electrode GT, a source electrode SD1 and a drain electrode SD2 respectively.

Each layer of orientation films ORI1 and ORI2, the transparent pixel electrode ITO1, the common transparent pixel electrode ITO2, a protective films PSV1 and PSV2 and an insulating film GI is formed inside the sealing material SL. Polarizing plates POL1 and POL2 are formed respectively on the outer surface of the lower transparent glass substrate SUB1 and the upper one SUB2.

The liquid crystal LC is poured between the lower orientation film ORI1 setting the direction of liquid crystal molecular and the upper orientation film ORI2, and sealed by the sealing portion SL.

The lower orientation film ORI1 is formed on the upper portion of the protective film PSV1 of the lower transparent glass substrate SUB1.

On the surface inside (liquid crystal LC side) the upper transparent glass substrate SUB2, the shielding film BM, the color filter FIL, the protective film PSV2, the common transparent pixel electrode ITO2(COM) and the upper orientation film ORI2 are laminated in order.

This liquid crystal display device is composed by forming respective layers on the side of the lower transparent glass substrate SUB1 separately from layers on the side of the upper transparent glass substrate SUB2, thereafter superimposing the upper transparent glass substrate SUB1 on the lower one SUB2, and sealing the liquid crystal LC between them.

《Thin film transistor TFT》

A thin film transistor TFT operates to reduce a channel resistance between a source and a drain when positive bias is applied to the gate electrode GT, and to increase the channel resistance when the bias is zero.

The thin film transistor TFT of each pixel is divided into three (plurality) in a pixel, and comprises a thin film transistors (divided thin film transistors) TFT1, TFT2 and TFT3. Thin film transistors TFT1 to TFT3 are respectively in the same size (the same channel length and width) substantially. These divided thin film transistors TFT1 to TFT3 respectively comprise mainly the gate electrode GT, the gate insulating film GI, I-type semiconductor layer AS made of I-type (intrinsic, a conductivity deciding impurity is not doped) non-crystalline silicon (Si), and a pair of a source electrode SD1 and a drain electrode SD2. Besides, because the source and the drain are essentially decided by a bias polarity between them and its polarity is reversed while operating in a

circuit of this liquid crystal display device, the understanding that the source and the drain are switched while operating is expected. However, in the following explanation, for convenience' sake, the fixed expression that one is a source, and the other is a drain is used.

《Gate electrode GT》

A gate electrode GT, as shown in detail in Figure 4 (a plan view wherein only a first conductive film g1, a second conductive film g2 and i-type semiconductor layer AS shown in Figure 2A are drawn), is constituted in the shape of jutting out in vertical direction (the upper direction in Figure 2-A and Figure 4) from the scanning signal line GL (branched out into T shape). The gate electrode GT is constituted so as to jut out to respective forming regions of thin film transistors TFT 1 to TFT 3. Respective gate electrodes GT of the thin film transistors TFT 1 to TFT3 are constituted integratedly (as a common gate electrode), and formed connected to the scanning signal line GL. The gate electrode GT is constituted by the first conductive film g1 of single layer not so as to make a large difference in level in a forming region of the thin film transistor TFT. The first conductive film g1 is formed using Chrome (Cr) film, for example, formed by sputtering, of which thickness is approximately 1000[Å].

This gate electrode GT is formed larger than the i-type semiconductor layer AS to be covered thoroughly (seeing from the lower side), as shown in Figure 2A, 2B and Figure 4. Therefore, in case of equipping a back light BL like as a fluorescent lamp below the lower transparent glass substrate SUB1, because the shadow of this gate electrode GT made of an opaque chrome should screen the i-type semiconductor layer AS from the light from the back light, a conductive phenomenon by light irradiation, that is to say, the deterioration of OFF characteristics of the thin film transistor TFT is not caused easily. Besides, the original size of the gate electrode GT, is the minimum (containing room for aligning the gate electrode GT with the source electrode SD1 and the drain electrode SD2) width which is necessary for the span from the source electrode SD1 to the drain electrode SD2, and the depth deciding a channel width W depends on the ratio of the depth and the distance (channel length) L between the source electrode SD1 and the drain electrode SD2, namely depends on a factor W/L deciding an interconductance gn.

Needless to say, the size of the gate electrode GT in this liquid crystal display device is larger than the original size above mentioned.

In addition to it, if it is considered on the function side of a gate and shielding of the gate electrode GT, the gate electrode GT and the scanning signal line GL can be formed integratedly on a single layer. In this case, aluminum (Al) containing silicon, pure aluminum, and aluminum containing palladium (Pd), etc. can be chosen as an opaque conductive material.

《Scanning signal line GL》

The scanning signal line GL is constituted a composite film comprising a first conductive film g1 and a second conductive film g2 formed on the first one. The first conductive film g1 of this scanning signal line GL is formed in the same manufacturing process as the first conductive film g1 of the gate electrode GT and constituted integratedly. The second conductive film g2 is formed using an aluminum film, for instance, formed by sputtering, of which thickness is approximately 1000 to 5500[Å]. The second conductive film g2 is constituted in order to reduce the resistivity of the scanning signal line GL, and to speed up the signal transmission (an improvement of the characteristics writing an information of a pixel).

Also, in the scanning signal line GL, the first conductive film g1 is wider than the second conductive film g2. That is to say, in the scanning signal line GL, the difference in level of the side wall of is gentle.

《Insulating film GI》

An insulating film GI is used as gate insulating films of respective thin film transistors TFT1 to TFT3. The insulating film GI is formed on the upper layer of the gate electrode GT and the scanning signal line GL. The insulating film GI is formed using a silicon nitride film, for instance, formed by plasma CVD, of which thickness is approximately 3000[Å].

《i-type semiconductor layer AS》

The i-type semiconductor layer AS, as shown in Figure 4, is used as channel forming regions of respective thin film transistors TFT1 to TFT3 divided into plurality. The i-type semiconductor layer AS is formed with a non-crystalline silicon film or a polycrystalline silicon film, of which thickness is approximately 1800[Å].

This i-type semiconductor AS is formed continuously by changing the ingredient of supplying gas after forming the insulating film GI used as the gate insulating film made of Si_2N_4 in the same plasma CVD apparatus, and without exposing the outside of the plasma CVD apparatus.

Also, a N^+ type semiconductor layer d0 (Figure 2B) wherein P for an ohmic contact is doped, is formed continuously in the same way, of which thickness is approximately 400[Å]. Thereafter, the lower transparent glass substrate SUB1 is taken out from the CVD apparatus, and the N^+ type semiconductor layer d0 and the i-type semiconductor layer AS are patterned into the independent island shape by photo processing technology, as shown in Figure 2A, 2B and Figure 4.

The i-type semiconductor layers AS, as shown in detail in Figure 2-A and Figure 4, are provided both sides of the crossover region (crossover potion) of the scanning signal line GL and the image signal line DL. The i-type semiconductor layer AS at this crossover portion is constituted in order to reduce the short-circuit of the scanning signal line GL and the image signal line DL at the crossover potion.

《Source electrode SD1 and drain electrode SD2》

Respective source electrode SD1 and drain electrode SD2 of the thin film transistors TFT1 to TFT 3 divided into plurality, as shown in detail in Figure 2A, 2B and Figure 5 (a plan view where only a first conductive film d1 to a third one d3 of Figure 2A are drawn), are provided on the i-type semiconductor layer AS separately.

The respective source electrode SD1 and the drain electrode SD2 comprises the lamination of the first conductive film d1, the second one d2 and the third one d3 in order from the lower layer side contacted with the N^+ type semiconductor layer d0. The first conductive film d1, the second one d2 and the third one d3 of the source electrode SD1 are formed in the same manufacturing process as the first one d1, the second one d2 and the third one d3 of the drain electrode SD2.

The first conductive film d1 is formed with a chrome film formed by sputtering, of which thickness is 500 to 1000[Å](approximately 600[Å] in this liquid crystal display device). When the chrome film is formed thick, stress is so increased that the film is formed within range of about 2000[Å] in thickness. The chrome film has good contact with the N^+ type semiconductor layer d0. The chrome film constitutes the so-called barrier layer preventing aluminum of the second conductive film d2 described later from diffusing to the N^+ type semiconductor layer d0. The first conductive film d1 can be formed with a high-melting point metal (Mo, Ti, Ta W) film, and a high-melting point metal silicide ($MoSi_2$, $TiSi_2$, $TaSi_2$, Wsi_2) film besides the chrome film.

After the first conductive film d1 is patterned by photo processing, the N^+ type semiconductor

layer d0 is removed using the same mask for photo processing or the first conductive film d1 as a mask. That is to say, the N^+ type semiconductor layer d0 remained on the i-type semiconductor layer AS except the first conductive film d1 is removed by self-alignment. In this case, because the N^+ type semiconductor layer d0 is etched to remove all in thickness direction, the surface of the i-type semiconductor layer AS is etched a little, of which degree can be controlled by an etching time.

Thereafter, the second conductive film d2 is formed with aluminum by sputtering, of which thickness is 3000 to 5500[Å] (approximately 3500[Å] in this liquid crystal display device). Because of small stress of an aluminum film compared with a chrome film, the aluminum film can be formed so thick that it is constituted to reduce the resistivity of the source electrode SD1, the drain electrode SD2 and the image signal line DL. The second conductive film d2 can be also formed with the aluminum film wherein silicon or copper (Cu) is contained as an additive, besides the aluminum film.

After patterning by the photo processing technology of the second conductive film d2, the third conductive film d3 is formed. The third conductive film d3 comprises a transparent conductive film (Indium-Tin-Oxide ITO: nesa film) formed by sputtering, and of which thickness is 1000 to 2000[Å] (approximately 1200[Å] in this liquid crystal display device). The third conductive film d3 comprises a transparent pixel electrode ITO1 as well as the source electrode SD1, the drain electrode SD2 and the image signal line DL.

The first conductive film d1 of the source electrode SD1 and that of the drain electrode SD2 are respectively extended into the inside (in a channel region) compared with the second conductive film d2 and the third conductive film d3 of the upper layer. That is to say, the first conductive films d1 in these portions are constituted to decide the gate length L of the thin film transistor TFT independent of the second conductive film d2 and the third conductive film d3.

The source electrode SD1 is connected to the transparent pixel electrode ITO1. The source electrode SD1 is constituted along the shape of difference in level of the i-type semiconductor layer AS (the difference in level equivalent in the total thickness of the first conductive film g1, the N^+ type semiconductor layer d0 and the i-type semiconductor layer AS). Concretely, the source electrode SD1 comprises the first conductive film d1 formed along the shape of difference in level

of the i-type semiconductor layer AS, the second conductive film d2 formed on the upper portion of the first conductive film d1, of which size of the side connected to the transparent pixel electrode ITO1 is smaller than the first conductive film d1, and the third conductive film d3 connected to the first conductive film d1 exposed from the second conductive film d2. The second conductive film d2 of the source electrode SD1 is constituted to get over the i-type semiconductor layer AS because the chrome film of the first conductive film d1 cannot be formed thick by the increase of the stress and cannot get over the shape of the difference in level of the i-type semiconductor layer AS. That is to say, the step coverage is improved by forming the second conductive film d2 thick. The second conductive film d2 can be formed so thick that it contributes to reduce to the resistivity of the source electrode SD1 (in the same way of the drain electrode SD2 and the image signal line DL). Because the third conductive film d3 cannot get over the difference in level caused by the i-type semiconductor layer AS of the second conductive film d2, it is constituted so as to connect to the exposed first conductive film d1 by making the size of the second conductive film d2 small. Because the first conductive film d1 and the third conductive film d3 not only have good adhesion, but also the difference in level of connected portion between them is small, the source electrode SD1 and the transparent pixel electrode ITO1 can be connected surely.

《Transparent pixel electrode ITO1》

The transparent pixel electrodes ITO1 are provided in each pixel, and constitutes one of a pixel electrode in the liquid crystal display portion. The transparent pixel electrode ITO1 is divided into three divided transparent pixel electrodes E1, E2 and E3 correspondent to respective thin film transistors TFT1 to TFT 3 divided into a plurality of pixels. The divided transparent pixel electrodes E1 to E3 are connected to source electrodes SD1 of respective thin film transistors.

The divided transparent pixel electrodes E1 to E3 are respectively patterned so as to be the same area substantially.

Thus, by dividing the thin film transistor TFT of one pixel into a plurality of the thin film transistors TFT1 to TFT 3, and connecting respective divided transparent pixel electrodes E1 to E3 to respective thin film transistors TFT 1 to TFT3 divided into the plurality, if one divided portion (for example, the thin film transistor TFT1) becomes a point defect, it is not regarded as a point defect judging from the whole pixel (the thin film transistors TFT 2 and TFT 3 are not defective).

Therefore, the probability causing the point defect can be reduced, and the defect can be difficult to see.

Besides, respective liquid crystal capacities Cpix comprising respective divided transparent pixel electrodes E1 to E3 and the common transparent pixel electrode ITO2 can be equal by constituting respective divided transparent pixel electrodes E1 to E3 in the same area substantially.

《Protective film PSV1》

A protective film PSV1 is provided on the thin film transistor TFT and the transparent pixel electrode ITO1. The protective film PSV1 is formed mainly to protect the thin film transistor TFT from moisture etc., and a film with high transparency and high moisture resistance is used. The protective film PSV1, for example, is formed with a silicon oxide film or a silicon nitride film formed by plasma CVD, of which thickness is approximately 8000[Å].

《Shielding film BM》

A shielding film BM is provided on the upper transparent glass substrate SUB2 so as to prevent an incident light from the outside (a light from the upper in Figure 2B) into the i-type semiconductor layer AS used as a channel forming region. The pattern of the shielding film BM is shown in hatching in Figure 6. Figure 6 is a plan view only drawing the third conductive film d3 made of an ITO film, a color filter FIL, and the shielding film BM in Figure 2A. The shielding film BM is formed, for example, with an aluminum film or a chromium film, etc. having high shield against the light. In this liquid crystal display device, a chrome film is formed by sputtering, of which thickness is approximately 1300[Å].

Therefore, the i-type semiconductor layers AS of the thin film transistors TFT1 to TFT3 are sandwiched with upper and lower shielding films BM and the slightly large gate electrode GT, of which portion is not irradiated by the external natural light and the back light. The shielding film BM is formed around the pixel, as shown in hatching portion in Figure 6, namely the shielding film BM is formed in lattice shape (black matrix), and the effective display region of one pixel is partitioned with this lattice. Therefore, an outline of each pixel is clear by the shielding film BM, and the contrast is improved. Namely, the shielding film BM has two functions that shielding against the i-type semiconductor layer AS and the black matrix.

Also, the lower transparent glass substrate SUB1 can be used as the observation side (the side

exposed to the outside) by equipping a back light with the upper transparent glass substrate SUB2.

《Common transparent pixel electrode ITO2》

A common transparent pixel electrode ITO2 is opposed to the transparent pixel electrode ITO1 provided in each pixel on the lower transparent glass substrate SUB1 side. The optical condition of the liquid crystal LC changes in response to the potential difference (electric field) between each pixel electrode ITO1 and the common transparent pixel electrode ITO2. This common transparent pixel electrode ITO2 is constituted in order that a common voltage V_{com} is applied. The common voltage V_{com} is an intermediate electric potential between low level driving voltage Vd_{min} applied to the image signal line DL and high level driving voltage Vd_{max}.

《Color filter FIL》

A color filter FIL is constituted by coloring with dye the dyeing base material made of resin material like as acrylic resin etc. The color filter FIL is formed per pixel in the shape of dot opposed to pixel (Figure 7), and is dyed in different colors (Figure 7 only shows the third conductive film layer d3 and the color filter FIL of Figure 3, and 45° , 135° cross hatch are conducted on each color filter FIL of R, G and B respectively). The color filter FIL is formed slightly large for covering the whole transparent pixel electrode ITO1 (E1 to E3) as shown in Figure 6, and the shielding film BM is formed inside the rim of the transparent pixel electrode ITO1 so as to be piled up on the edge of the color filter FIL and the transparent pixel electrode ITO1.

The color filter FIL can be formed to the following. First, the dyeing base material is formed on the surface of the upper transparent glass substrate SUB2, and the dyeing base material except red filter forming region is removed by photolithography technology. Thereafter, the dyeing base material is dyed with a red dye, a fixation processing is performed, and a red filter R is formed. Then, a green filter G and a blue filter B are formed in order by performing the same processing.

《Protective film PSV2》

A protective film PSV2 is provided to prevent the dye which dyes the color filter FIL in different colors from leaking into the liquid crystal LC. The protective film PSV2 is formed, for example, with transparent resin material such as acrylic resin, epoxy resin, etc.

《Pixel arrangement》

Each pixel of the liquid crystal display portion, as shown in Figure 3 and Figure 7, is provided plurally in the same row direction as the scanning signal line GL extends, and constitutes respective pixel rows X1, X2, X3, X4 .... Respective pixels of each pixel row X1, X2, X3, X4...constitute the same arrangement of the thin film transistors TFT1 to TFT3 and the divided transparent pixel electrodes E1 to E3. That is to say, respective pixels of odd pixel rows X1, X3, ...have the constitution, wherein the thin film transistors TFT 1 to TFT 3 are provided in left side, and the divided transparent pixel electrodes E1 to E3 are provided in right side. Respective pixels of even pixel rows X2, X4, ...adjacent to respective line direction of add pixel rows X1, X3, ...are constituted symmetrically with the pixel that respective pixels of the odd pixel rows X1, X3, ... are turned over on the basis of the direction that the image signal line DL extends. That is to say, respective pixels of the pixel rows X2, X4, ... have the constitution, wherein the thin film transistors TFT1 to TFT3 are provided in right side, and the transparent pixel electrodes E1 toE3 are provided in left side. Respective pixels of the pixel rows X2, X4, ... are provided in the condition to be moved (shifted) by a half pitch of a pixel to the row direction against respective pixels of the pixel rows X1, X3, ... That is to say, when each pixel pitch of the pixel row X is 1.0 (1.0 pitch), the next pixel row X, of which each pixel pitch is 1.0, is shifted by 0.5 pixel pitch (0.5 pitch) in the row direction against the previous pixel row X. The image signal line DL which extends to the row direction between each pixel is constituted so as to extend in the row direction by a half pitch of a pixel (0.5 pitch) between each pixel row X.

Consequently, as shown in Figure 7, a pixel wherein the decided color filter of the previous pixel row X is formed (for example, a pixel wherein a red filter R of the pixel row X3 is formed) separates from a pixel wherein the same one color filter of the next pixel row X is formed (for example, a pixel wherein a red filter R of the pixel row X4 is formed) at intervals of 1.5 pixel (1.5 pitch), and color filters FIL of RGB are a triangle provision. Because the triangle provision structure of RGB of the color filter FIL enables to mix each color well, the resolution of the color image can be improved.

Also, the image signal line DL extends only to an interval of half pixel in the direction of row between each pixel row X, so that it does not cross the adjacent image signal line DL. Therefore, an occupation area can be reduced by getting rid of leading wires of the image signal line DL, and

also a multi layered interconnection structure can be disused by getting rid of detour of the image signal line DL.

《Display device whole equivalent circuit》

An equivalent circuit of this liquid crystal display device is shown in Figure 8. XiG, Xi + 1G, ... are the image signal line DL connected to a pixel wherein a green filter G is formed. XiB, Xi + 1B, ... is the image signal line DL connected to a pixel wherein a blue filter B is formed. Xi + 1R, Xi + 2R, ... is the image signal line DL connected to a pixel wherein a red filter R is formed. These image signal lines DL are selected by an image signal driving circuit. Yi is a scanning signal line GL selecting a pixel row X1 shown in Figure 3 and Figure 7. In the same way, respective Yi + 1, Yi + 2, ... are the scanning signal line GL selecting respective pixel rows X2, X3, ... These scanning signal lines GL are connected to vertical scanning circuits.

《Structure of storage capacity element Cadd》

Respective divided transparent pixel electrodes E1 to E3 are formed bent to L shape so as to overlap the adjacent scanning signal line GL, at the terminal connected to the thin film transistor TFT and the opposed terminal. This overlap constitutes, as obvious from Figure 2C, a storage capacity element (electrostatic capacity element) Cadd wherein respective divided transparent pixel electrodes E1 to E3 is one electrode PL2, and the adjacent scanning signal line GL is the other electrode PL1. An inductive film of this storage capacity element Cadd is constituted by the same layer as an insulating film GI used as a gate insulating film of the thin film transistor TFT.

The storage capacity element Cadd, as obvious from Figure 4, is formed in the region where the first conductive film g1 of the gate line GL is widened. Beside, the portion of the first conductive film g1 crossed with the image signal line DL is narrow to reduce the probability causing short circuit of the image signal line DL.

In a portion between respective divided transparent pixel electrodes E1 to D3 overlapped to constitute the storage capacity element Cadd and the electrode PL1, in the same way as the source electrode SD1, an island region comprising the first conductive film d1 and the second conductive film d2 is provided so as to disconnect the transparent pixel electrode ITO1 in getting over the difference in level. This island region is constituted as small as possible not to reduce the area of the transparent pixel electrode ITO1 (aperture ratio).

《Equivalent circuit of a storage capacity element Cadd and its operation》

An equivalent circuit of pixel shown in Figure 2A is shown in Figure 9. In Figure 9, Cgs is a parasitic capacity formed between the gate electrode GT and the source electrode SD1 of the thin film transistor TFT. An inductive film of the parasitic capacity Cgs is the insulating film GI. Cpix is a liquid crystal capacity formed between the transparent pixel electrode ITO1 (PIX) and the common transparent pixel electrode ITO2 (COM). Inductive films of the liquid crystal capacity Cpix is a liquid crystal LC, the protective film PSV1, and the orientation films ORI1 and ORI2. Vlc is a middle point electric potential.

The storage capacity element Cadd works to reduce an influence of the gate electric potential transition ΔVg against the middle point electric potential (pixel electrode electric potential) V1c. The following expression shows this situation.

$$\Delta V1c=(Cgs/(Cgs+Cadd+Cpix) \times \Delta Vg$$

$\Delta V1c$ shows a transition of middle point electric potential by ΔVg. This transition $\Delta V1c$ is a cause of DC current constituent added to the liquid crystal LC, and the larger the storage capacity Cadd is, the more the value is reduced. Also, the storage capacity element Cadd has a function to lengthen the discharge time, and stores for a long time the image information after the thin film transistor TFT is off. Reduction of DC current constituent applied to the liquid crystal LC improves a lifetime of the liquid crystal LC, and can reduce so-called burn that a previous image remains at switching the liquid crystal display.

As above mentioned, because the gate electrode GT is formed slightly large so as to cover I-type semiconductor layer AS thoroughly, an overlapped area of the source electrode SD1 and the drain electrode SD2 is increased. Therefore, the parasitic capacity Cgs becomes large, an adverse effect that the middle point electric potential V1c is influenced easily by a gate (scanning) signal Vg is caused. However, this demerit can be solved by providing the storage capacity element Cadd.

A storage capacity of the storage capacity element Cadd is set about four times to eight times ($4 \cdot Cpix<Cadd<8 \cdot Cpix$) for the liquid crystal capacity Cpix, and eight times to thirty-two times ($8 \cdot Cgs<Cadd<32 \cdot Cgs$) for the superposition capacity Cgs, from the writing characteristics of pixel.

《Wire connection of the storage capacity element Cadd electrode line》

The last scanning signal line GL used only as the capacity electrode line (or the first scanning

signal line GL), as shown in Figure 8, is connected to the common transparent pixel electrode ITO2 (Vcom). The common transparent pixel electrode ITO2, as shown in Figure 2B, is connected to the outer leading interconnection with silver paste material SL at the rim of the liquid crystal display device. Besides, conductive layers (g1 and g2) that the portion of this outer leading interconnection are constituted in the same manufacturing process as the scanning signal line GL. As a result, the last scanning signal line (capacity electrode line) GL can be connected to the common transparent pixel electrode ITO2 easily.

As shown by dot line in Figure 8, the scanning signal line (capacity electrode line) GL of the last line (the first line) can be also connected to the scanning signal line GL of the first line (the last line). Besides, this connection can be conducted by the inner interconnection or the outer leading interconnection inside the liquid crystal display portion.

《DC current constituent offset by scanning signal of storage capacity element Cadd》

This liquid crystal display device, based on DC current offset system (DC cancel system) described in Japanese Patent Laid-open Sho. 62-95125 previously applied by the present applicant, as shown in Figure 10 (time chart), can further reduce DC current constituent added to the liquid crystal LC by controlling a driving voltage of the scanning signal line GL. In Figure 10, Vi is a driving voltage of random scanning signal line GL, and Vi + 1 is a driving voltage of the next scanning signal line GL. V_{ee} is a low level driving voltage $V_{d\,min}$ applied to the image signal line DL, and V_{dd} is a high level driving voltage $V_{d\,max}$ applied to the image signal line DL. Voltage transitions $\Delta V1$ to $\Delta V4$ of the middle point electric potential Vlc (see Figure 9) at each time t = t1 to t4 are shown by the next expressions, as the total capacity C of pixel = Cgs + Cpix + Cadd.

$\Delta V1 = -(Cgs/C) \cdot V2$

$\Delta V2 = +(Cgs/C) \cdot (V1 + V2) - (Cadd/C) \cdot V2$

$\Delta V3 = -(Cgs/C) \cdot V1 + (Cadd/C) \cdot (V1 + V2)$

$\Delta V4 = -(Cadd/C) \cdot V1$

When the driving voltage applied to the scanning signal line GL is enough (see [notes] below), DC voltage applied to the liquid crystal LC is shown by the next expression.

$\Delta V3 + \Delta V4 = (Cadd \cdot V2 - Cgs \cdot V1)/C$

Therefore, in case of $Cadd \cdot V2 = Cgs \cdot V1$ is, DC voltage added to the liquid crystal LC is 0.

[notes] Though a transition of the driving voltage Vi at t1 and t2 affects on the middle point electric potential Vlc, the middle point electric potential Vlc is made the same electric potential as the image signal electric potential through the signal line Xi during t2 to t3 (enough writing of the image signal). The electric potential added to the liquid crystal LC is almost decided by the electric potential right after the thin film transistor TFT is OFF (OFF term of the thin film transistor TFT is much longer than ON term). Therefore, a calculation of DC current added to the liquid crystal LC does not need being taken into consideration during t1 to t3, and the electric potential right after the thin film transistor TFT is OFF, that is to say, an influence of transition period at time of t3 and t4 needs to be considered. Besides, the polar character of the image signal is inverted per frame or per line, and the DC current constituent by the image signal itself is zero.

Namely, the DC current offset system can push up lowering by pulling of the middle point electric potential Vlc by the parasitic capacity Cgs by the driving voltage applied to the storage capacity element Cadd and the scanning signal line (capacity electrode line) GL of the next line, and reduce extremely the DC current constituent added to the liquid crystal LC. As a result, the liquid crystal display device can improve a lifetime of the liquid crystal LC. Of course, in case that the gate electrode GT is enlarged to improve a shielding effect, the storage capacity of the storage capacity element Cadd should follow it.

Then, a manufacturing method of a color liquid crystal display device concerning this invention is explained with Figure 1A. A chrome film of 1300[Å] in thickness is firstly formed on the upper transparent glass substrate SUB2 by sputtering. Then, a masking film BM is formed by etching the chrome film selectively by photolithography using nitric acid second cerium ammonium solution as an etching solvent. Next, a dyeing base material is provided on the masking film BM, and the dyeing base material except a red filter forming region is removed by photolithography. A red color filter FIL (R) is formed by dyeing a dyeing base material with a red dye, and performing a fixation processing. Next, a dyeing base material is provided, and the dyeing base material except a green filter forming region is removed by photolithography. A green color filter FIL (G) is formed by dyeing the dyeing base material with a cyan dye, furthermore dyeing the same dyeing base material with a yellow dye, and performing a fixation processing. Then, a dyeing base material is provided, and the dyeing base material except a blue

filter forming region is removed by photolithography. Then, a blue color filter FIL (B) is formed by dyeing the dyeing base material with a blue dye, and performing a fixation processing.

In this manufacturing method of the color liquid crystal display device, the green color filter FIL (G)is formed by dyeing the dyeing base material with the cyan dye, and furthermore dyeing the same dyeing base material with the yellow dye. Therefore, the green color filter FIL (G) can be dyed easily to the prescribed color tone because each dyeing quantity of the cyan dye and the yellow dye to the dyeing base material can be constant by fixing each dyeing condition of the cyan dye and the yellow dye.

Other manufacturing method of a color liquid crystal display device concerning this invention is explained with Figure 1B. First, a masking film BM is formed on the upper transparent glass substrate SUB2. A dyeing base material is provided on the masking film BM, a resist RST is coated on the dyeing base material. After the resist RST of a red filter forming region is removed by photolithography, an exposed portion of the dyeing base material is dyed with a red dye. Then, the resist RST is removed, and the resist RST is coated on the dyeing base material. After the resist RST of a green filter forming region is removed by photolithography, an exposed portion of the dyeing base material is dyed with a cyan dye, furthermore the same portion of the dyeing base material is dyed with a yellow dye. The resist RST is removed, and the resist RST is coated on the dyeing base material. After the resist RST of a blue filter forming region by photolithography, an exposed portion of the dyeing base material is dyed with a blue dye. After the resist RST is removed, the red color filter FIL (R), the green color filter FIL (G) and the blue color filter FIL (B) are formed by performing a fixation.

The invention by the present inventors is explained above concretely based on said embodiment, however, needless to say, this invention is not limited to said embodiment, and is possible to vary within range of the substance.

For instance, in above embodiment, a reverse stagger structure: gate electrode formation → gate insulating film formation →semiconductor layer formation → source / drain electrode formation, is shown. However, this invention is effective in a stagger structure that the order of up and down relation or the formation is reverse.

【Effect】

As above mentioned, in this manufacturing method of the liquid crystal display device concerning this invention, because each dyeing quantity of the cyan dye and the yellow dye to the dyeing base material can be constant by fixing each dyeing condition of the cyan dye and the yellow dye, a green color filter can be dyed easily in prescribed color tone. In this way, the effect of this invention is remarkable.

4. A brief explanation of Figures

Figure 1A and 1B explain respective manufacturing methods of color liquid crystal display devices concerning this invention. Figure 2A is a plan view of the main portion showing one pixel of the liquid crystal display portion of the active matrix system color liquid crystal display device wherein this invention is applied. Figure 2B is a cross sectional view of the portion cut by the cutting line ⅡB-ⅡB of Figure 2A and the periphery of sealing portion. Figure 2C is a cross sectional view on the cutting line ⅡC-ⅡC of Figure 2A. Figure 3 is a plan view of the main portion of the liquid crystal display wherein a plurality of pixels shown in Figure 2A are provided. Figure 4 to Figure 6 are plan views drawing only the decided layer of pixels shown in Figure 2A. Figure 7 is a plan view of the main portion drawing only the pixel electrode layer and the color filter layer shown in Figure 3. Figure 8 is an equivalent circuit diagram showing the liquid crystal display of the active matrix system color liquid crystal display device. Figure 9 is an equivalent circuit diagram of the pixel described in Figure 2A. Figure 10 is a time chart showing driving voltage of the scanning signal line by DC current offset system.

SUB...transparent glass substrate

GL...scanning signal line

DL...image signal line

GI...insulating film

GT...gate electrode

AS...I-type semiconductor layer

SD...source electrode or drain electrode

PSV...protective film

BM...shielding film

LC...liquid crystal

TFT...thin film transistor

ITO...transparent pixel electrode

G, d...conductive film

Cadd...storage capacity element

Cgs...parasitic capacity

Cpix...liquid crystal capacity